TITLE OF THE INVENTION

INTERPOSER SUBSTRATES WITH MULTI-SEGMENT INTERCONNECT SLOTS, SEMICONDUCTOR DIE PACKAGES INCLUDING SAME, SEMICONDUCTOR DICE FOR USE THEREWITH AND METHODS OF FABRICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of application Serial No. 10/409,804, filed April 9, 2003, ~~pending~~. NOW US PATENT NO. 7,102,217

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The present invention relates generally to fabrication of semiconductor devices and, more specifically, to the packaging of semiconductor dice.

[0003] State of the Art: In the field of semiconductor device manufacture, testing and packaging of various types of semiconductor dice are conducted in a similar manner. Thus, conventional dynamic random access memory dice (DRAM's), static random access memory dice (SRAM's), programmable memory dice (PROM's, EPROM's, EEPROM's, flash memories), logic dice, and microprocessor dice are fabricated, tested and packaged in a generally similar manner.

[0004] Following fabrication of a plurality of dice on a wafer or other bulk substrate of semiconductor material, a cursory test for functionality is conducted on each die, such as by probe testing. The dice are then singulated, and those passing the functionality test are picked from the wafer, typically for packaging, such as by transfer molding, and subsequent incorporation into a higher-level assembly. Typically, each die is formed with one or more rows of bond pads on the active surface. The bond pad row or rows may be formed along a central axis of the die or along one or more peripheral portions thereof. Transfer molded packages may comprise bond wires which electrically couple bond pads on the die to leads of a lead frame, the outer ends of the leads extending beyond the protective encapsulant, which is typically a silicon-